line 17, cancel "1" and substitute -- 1a --;

line 31, after "103-3,C" add -- (not shown) --;

line 36, after "103-12,C" add -- (not shown) --.

Page 9, line 20, between "102" and "than" add -- and PIC holes 104 --.

Page 10, line 13, change "P1C" to -- PIC --.

Page 10, line 33, cancel "selective" and substitute -- selected --.

Page 11, line 9, cancel "components" and substitute -- component --.

Page 14, line 6, cancel "component";

line 6, between "conductive" and "holes" add -- component --.

Page 16, line 12, between "columns" and "cells" add -- of --.

Page 17, line 8, cancel "606-1, 1" and substitute -- 606-1,1 --;

line 29, cancel "length" and substitute -- lengths --.

Page 19, line 24, between "addition" and "vertical" add -- the --;

line 24, between "lead" and "is" add -- 629-1 --;

line 31, cancel "devised" and substitute -- desired --.

Page 20, line 19, cancel "lead" (second occurrence) and substitute -- leads --;

line 21, cancel "as";

line 23, between "structure" and "6d" add -- of Figure --.

Page 21, line 3, cancel "are" and substitute -- is --;

line 16, change "testport" to -- test port --;

line 17, cancel "are" and substitute -- is --.

Page 22, line 10, cancel "is" and substitute -- are --;

line 15, between "applies" and "to" add -- a voltage --;

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MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233

line 16, cancel "Vpp over 2" and substitute -- Vpp/2 --.

Page 23, line 9, cancel "605B" and substitute -- 605b --;

line 15, between "chip" and "contains" add -- which --;

line 31, after "8b" insert -- , which consists of Figures 8b1 and 8b2, --.

Page 25, line 6, as two paragraphs, insert

-- Figure 9 illustrates how an electronic system utilizing the programmable PC board of this invention is designed. As indicated in Figure 9, the designer first creates a computer model of the board in a computer aided design system. The designer then simulates placement of models of the desired electronic components, be they discrete elements, memory, logic gates, or microprocessors, on selected component contacts on the board and simulates the interconnection of these electronic components using the standard PC board of this invention together with the programmable interconnect chip or chips of this invention. The computer then simulates the electrical performance of the system with the electrical components so placed and interconnected and indicates whether or not the configuration selected by the designer yields the desired electronic function. The designer has choices in the placement of the electronic components on the programmable PC board and in their interconnection but is assisted in

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SILBERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233

this placement by certain logical rules in the computer aided design program.

Algorithms for use in computer aided design systems of the type required to implement the design of electronic systems utilizing this invention are currently available in the electronic design industry. Examples of algorithms for partitioning and placement of the electronic components on the programmable PC board of this invention are described in (a) Lauther, "A Min-Cut Placement Algorithm for General Cell Assemblies Based on a Graph Representation," 16th Design Automation Conf., June 25 - 27, 1979, pp. 1 - 10, reprinted in Comp. Paps. Design Automation Conf., 1988, pp. 182 - 191, and (b) Fiduccia et al, "A Linear-Time Heuristic for Improving Network Partitions," 19th ACM/IEEE Design Automation Conf., June 14 - 16, 1982, pp. 175 - 181 reprinted in ibid., pp. 241 - 247. Examples of algorithms for routing of the programmable interconnect chip(s) are described in (c) Marek-Sadowska, "Two Dimensional Router for Double Layer Layout," 22nd ACM/IEEE Design Automation Conf., June 23 - 26, 1985, pp. 117 - 123, (d) Tzeng et al, "Codar: A Congestion-Directed General Area Router," IEEE Int'l Conf. on CAD, Nov. 7 - 10, 1988, pp. 30 - 33, (e) Lin et al, "A Detailed Router Based on Simulated Evolution," ibid., pp. 38 - 41, and (f) Lee et al, "A New Global Router

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& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233

for Row-Based Layout," ibid., pp. 180 - 183. --.

IN THE CLAIMS

Rewrite Claims 20 and 21 as given below:

--20. (Amended) Structure comprising a printed circuit board and a [A] programmable interconnect chip for use in interconnecting electronic components formed on said [a] printed circuit board, said chip comprising:

a first set of conductive leads formed in a first direction across the surface of said chip, [each of said conductive leads comprising one or more conductive segments,] portions of selected ones of said conductive leads [segments] being connected to pads on the surface of said programmable interconnect chip, each of said pads being adapted for contact to a corresponding contact on said [the] printed circuit board;

a second set of conductive leads [conductors] formed on said programmable interconnect chip in a second direction not parallel to said first direction, at least one [each] conductive lead in at least one of said first and second sets [set] of conductive leads comprising two [one] or more segments; and

means for programmably electrically interconnecting selected ones of said conductive leads in said first set of conductive leads to one or more of said conductive leads in said second set of conductive leads.

21. (Amended) Structure as in Claim 20 wherein said programmable interconnect chip further includes [comprises]:

programmable transistors [active transistor] in said programmable interconnect chip;

means for electrically connecting selected ones of the segments of conductive leads in said first set of conductive leads and in said second set of conductive leads to

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SKJERVEN, MORRILL,
MacPHERSON, FRANKLIN
& FRIEL

25 METRO DRIVE
SUITE 700
SAN JOSE, CA 95110
(408) 283-1222
FAX (408) 283-1233